DEMO MANUAL DC1477A

LTM4609EV: $36 \mathrm{~V}_{\mathrm{IN}}, 34 \mathrm{~V}_{\text {OUt }}$ Buck-Boost DC/DC $\mu$ Module ${ }^{®}$ Regulator

## DESCRIPTION

Demonstration circuit DC1477A features the LTM ${ }^{\circledR} 4609 E V$, a high voltage, high efficiency, high density switch mode buck-boost power module. The LTM4609EV regulates an output voltage above, below or equal to the input voltage. DC1477A accepts an input voltage from 10V to 36V with a preset output voltage of 30 V at up to 3 A . Derating may be necessary for certain $\mathrm{V}_{\text {IN }}, \mathrm{V}_{\text {OUT }}$ and thermal conditions. An input $\pi$ filter option is included on the DC1477A to minimize the input ripple. The switching frequency may be synchronized to an external clock from 200 kHz to

400 kHz to reduce undesirable frequency harmonics and/ or parallel multiple modules for even higher output current. The LTM4609 data sheet must be read in conjunction with this demo manual prior to working on or modifying demo circuit DC1477A

Design files for this circuit board are available at http://www.linear.com/demo
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## PGRFORMAOCE SUMMARY $\left(\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}\right)$

| PARAMETER | CONDITION | VALUE |
| :--- | :--- | :--- |
| Minimum Input Voltage |  | 10 V to 36 V |
| Output Voltage $\mathrm{V}_{\text {OUT }}$ |  | $30 \mathrm{~V} \pm 2 \%$ |
| Maximum Continuous Output Current | Derating is Necessary for certain $\mathrm{V}_{\text {IN }}, \mathrm{V}_{\text {OUT }}$ and <br> Thermal Conditions | $3 \mathrm{~A} \mathrm{DC} \mathrm{at} 10 \mathrm{~V}_{\text {IN }}$ <br> 8 A DC at 24 V <br> $10 \mathrm{~A} \mathrm{DC} \mathrm{at} \mathrm{V}_{\text {IN }}>30 \mathrm{~V}$ |
| Default Operating Frequency |  | 300 kHz |
| Efficiency | $\mathrm{V}_{\text {IN }}=20 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=30 \mathrm{~V}, \mathrm{I}_{\text {OUT }}=3 \mathrm{~A}$ | $96.7 \%$, See Figure 3 for More Information |

BOARD PHOTO


## DEMO MANUAL DC1477A

## PUICK START PROCEDURE

Demonstration circuit DC1477A is an easy way to evaluate the performance of the LTM4609EV. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions for a typical $30 V_{\text {OUT }}$ application:

| RUN | CLOCK | MODE | START |
| :---: | :---: | :---: | :---: |
| ON | PROG | CCM | SSO |

2. With the power supply off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0 A and $\mathrm{V}_{\text {IN }}$ supply between 10 V to 36 V .
3. Turn on the power at the input. The output voltage should be $30 \mathrm{~V} \pm 2 \%$.
4. Once the proper output voltage is established, adjustthe load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters. A cooling fan and heat sink are necessary for $\mathrm{V}_{\text {IN }}<10 \mathrm{~V}$ and $\mathrm{I}_{\text {OUT }}=3 \mathrm{~A}$.
5. To measure input and output ripple, please refer to Figure 2 for proper setup.
6. To adjust the switching frequency turn off the power supply and modify R6 and R7. Do not allow voltage at pin PLLFLTR to exceed 2.4V.
7. Inductor and RSENSE should be modified to accommodate certain input and output condition. Refer to the data sheet for details.
8. The input filter formed by CIN2, L2 and L3, CIN3 and CIN4 is for the purpose of reducing the input voltage ripple. The magnetic beads L 2 and L 3 are not necessary, but they help to reduce the high frequency ringings on the input supply significantly. See Figure 5 for details.
9. The optional components Rsnb1 and Csnb1, Rsnb2 and Csnb2 can be used to form RC snubber circuits on the switching nodes, which may help to reduce the output ripple. Refer to the data sheet for details.

## PUICK START PROCEDURE



Figure 1. Test Setup of DC1477A


Input or Output Capacitor
Figure 2. Proper Scope Probe Placement for Measuring Input or Output Ripple

## DEMO MANUAL DC1477A

## DUICK START PROCEDURE



Figure 3. Measured Efficiency at Different $V_{I N}$

## PUICK START PROCEDURE


$\mathrm{V}_{\text {IN }}=10 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=30 \mathrm{~V}$, CCM Mode
1.5A to 3A Load Step
$\mathrm{C}_{\text {OUT }}=2 \times 10 \mu \mathrm{~F}$ Ceramic $+2 \times 100 \mu \mathrm{~F}$ Alum

$\mathrm{V}_{\text {IN }}=36 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=30 \mathrm{~V}$, CCM Mode
1.5A to 3A Load Step
$\mathrm{C}_{\text {OUT }}=2 \times 10 \mu \mathrm{~F}$ Ceramic $+2 \times 100 \mu \mathrm{~F}$ Alum

Figure 4. Measured Load Transient Response (1.5A Step, 50\% to 100\%)

$V_{\text {IN }}=10 \mathrm{~V}, \mathrm{~V}_{\text {OUT }}=30 \mathrm{~V}, I_{\text {OUT }}=3 \mathrm{~A}$
W/O Input Filter: Short L2 and L3, Remove $\mathrm{C}_{\mathrm{IN} 2}$
$\mathrm{V}_{\text {IN }}$ Peak-to-Peak Ripple $=2.78 \mathrm{~V}$

$V_{I N}=10 \mathrm{~V}, V_{\text {OUT }}=30 \mathrm{~V}, I_{\text {OUT }}=3 \mathrm{~A}$
W Input Filter: Stuff L2, L3 and $\mathrm{C}_{\text {IN2 }}$
$\mathrm{V}_{\text {IN }}$ Peak-to-Peak Ripple $=0.47 \mathrm{~V}$

Figure 5. Input Voltage Ripple Measured at $\mathrm{C}_{\mathrm{IN} 1}$ with 300 MHz BW Probe, with and without the Input Filter

## DEMO MANUAL DC1477A

## PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
| :---: | :---: | :---: | :---: | :---: |
| Required Circuit Components |  |  |  |  |
| 1 | 1 | CSS | CAP., X7R, 0.1 $\mu$ F, 25V, 10\%, 0603 | AVX, 06033C104KAT4A |
| 2 | 1 | CIN1 | CAP., ALUMINUM, 100 ${ }^{\text {F }}$, 20\%, 50V | SANY0, 50ME100WX+TS (now SUNCON 50ME100WX) |
| 3 | 2 | C03, C04 | CAP., X7R, 10 ${ }^{\text {F }}$, 35V, 10\%, 1210 | MURATA, GRM32ER7YA106KA12L |
| 4 | 3 | CIN2, CIN3, CIN4 | CAP., X7R, 4.7 $\mu \mathrm{F}, 50 \mathrm{~V}, 10 \%$, 1206 | Taiyo Yuden, UMK316BJ475KL-T |
| 5 | 2 | C05, C06 | CAP., ALUMINUM, 100 ${ }^{\text {F }}$, 35V | SANYO, 35HVH100M (now SUNCON 35HVH100M) |
| 6 | 1 | L1 | IND. POWER IND, 3.3 ${ }^{\text {H }}$ | VISHAY, IHLP5050FDER3R3M01 |
| 7 | 1 | R1 | RES., CHIP, 100k, 1/16W, 5\%, 0603 | VISHAY, CRCW0603100KJNEA |
| 8 | 1 | R5 | RES., CHIP, 2.74k, 1/16W, 1\%, 0603 | VISHAY, CRCW06032K74FKEA |
| 9 | 1 | R6 | RES., CHIP, 4.64k, 1/16W, 1\%, 0603 | VISHAY, CRCW06034K64FKEA |
| 10 | 1 | R7 | RES., CHIP, 1.21k, 1/16W, 1\%, 0603 | VISHAY, CRCW06031K21FKEA |
| 11 | 2 | RS1,RS2 | RES., CHIP, 0.015 $1 / 2 \mathrm{~W}, 1 \%, 1206$ | IRC, LRC-LRF1206-01-R015-F |
| 12 | 1 | U1 | $\begin{aligned} & \text { I.C., LTM4609EV\#PBF, } \\ & 15 \mathrm{~mm} \times 15 \mathrm{~mm} \times 2.8 \mathrm{~mm} \text { LGA } \end{aligned}$ | LINEAR TECH., LTM4609EV\#PBF |

## Additional Demo Board Circuit Components

| 1 | 0 | CIN5, Csnb1, Csnb2 (OPT) | CAP., 1206 |  |
| :---: | :--- | :--- | :--- | :--- |
| 2 | 0 | C2, C4, C5, CP, CFF (OPT) | CAP., 0603 | $50 \mathrm{ME} 100 \mathrm{WX}+$ TS |
| 3 | 0 | C01, CO2 (OPT) | CAP., SVP, 100 $\mu$ F, D3L |  |
| 4 | 0 | C07 (OPT) | CAP., 1206, 35V |  |
| 5 | 0 | C08 (OPT) | POSCAP, D3L |  |
| 6 | 2 | D1, D2 | ZENER DIODE,4.7V | Central Semi., CMDZ5230B-7-F |
| 7 | 2 | L2, L3 | IND. POWER IND, 0.4 $4 \mathrm{H}, 1806$ | Fair-Rite, 2518065007Y6 |
| 8 | 1 | R2 | RES., CHIP, 51k, $1 / 16 \mathrm{~W}, 5 \%, 0603$ | VISHAY, CRCW060351KOJNEA |
| 9 | 1 | R8 | RES., CHIP, 20k, $1 / 16 \mathrm{~W}, 1 \%, 0603$ | VISHAY, CRCW060320KOFKEA |
| 10 | 0 | RS3, Rsnb1, Rsnb2 (OPT) | RES.,1206 |  |
| 11 | 0 | R9, RUVLO (OPT) | RES., 0603 |  |

## Hardware: For Demo Board Only

| 1 | 2 | JP1, JP2 | 2MM SINGLE ROW HEADER, 3-PIN | SAMTEC, TMM-103-02-L-S |
| :---: | :---: | :--- | :--- | :--- |
| 2 | 2 | JP3, JP4 | 2MM SINGLE ROW HEADER, 4-PIN | SAMTEC, TMM-104-02-L-S |
| 3 | 4 | JP1, JP2, JP3, JP4 | SHUNT | SAMTEC, 2SN-BK-G |
| 4 | 10 | TP1, TP4, TP5, TP7, TP9, <br> TP11-TP15 | TESTPOINT, TURRET, 0.095" | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| 5 | 4 | TP2, TP3, TP8, TP10 | BANANA JACK, | KEYSTONE, 575-4 |
| 6 | 4 | STAND OFF | STAND-OFF, NYLON 0.50" TALL | KEYSTONE, 8833 (SNAP 0N) |

## SCHEMATIC DIAGRAM



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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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